AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application;

Claim 1. (Canceled)

Claim 2. (Currently Amended) ~~The~~ A sampling frequency conversion apparatus ~~according to claim 1~~ for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read-out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an address difference between a writable address and a readable address in said storage means; and

address control means for performing an optimization operation optimizing the address difference detected by said address difference detecting means, wherein

said address control means adaptively sets a limitation on the optimizing operation, wherein

said address control means works so as not to execute the optimization operation when the address difference detected by said address difference detecting means falls within a predetermined range after passage of a predetermined

period of time from a starting time when the input data is supplied.

Claim 3. (Currently Amended) ~~The~~ A sampling frequency conversion apparatus ~~according to claim~~ for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read-out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an address difference between a writable address and a readable address in said storage means; and

address control means for performing an optimization operation optimizing the address difference detected by said address difference detecting means, wherein

said address control means adaptively sets a limitation on the optimizing operation, wherein

said address control means works so as not to execute the optimization operation when the address difference detected by said address difference detecting means falls within a predetermined range after passage of a predetermined period of time from a time when the power source circuit is switched on.

Claim 4. (Currently Amended) ~~The~~ A sampling frequency

conversion apparatus ~~according to claim 1~~ for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read-out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an address difference between a writable address and a readable address in said storage means; and

address control means for performing an optimization operation optimizing the address difference detected by said address difference detecting means, wherein

said address control means adaptively sets a limitation on the optimizing operation, wherein

said predetermined period of time is longer than a time required for stabilizing a ratio between the first sampling frequency of the input data and the second sampling frequency of the output data after a start of supplying said input data.

Claims 5 and 6. (Canceled)

Claim 7. (Currently Amended) ~~The~~ A sampling frequency conversion apparatus ~~according to claim 6~~for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read-out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an address difference between a writable address and a readable address in said storage means; and

address control means for performing an optimization operation optimizing the address difference detected by said address difference detecting means, wherein

said address control means adaptively sets a limitation on the optimizing operation, wherein

said address control means performs a control operation to bring said address difference close to a predetermined optimum value imposing no limitation when a predetermined period of time has not been passed after a start of supplying said input data or when the address difference detected by said address difference detector means falls outside of a predetermined range, wherein

said address control means executes the control operation by bringing the address difference close to the predetermined optimum value by judging that a moment at which the changing address difference value exceeds the predetermined optimum value or becomes smaller than the predetermined optimum value, is the moment of an optimum address difference.

Claim 8. (Currently Amended) A sampling frequency conversion apparatus having a plurality of sampling frequency conversion means for converting a first sampling frequency of input data into ~~a second~~ a second sampling frequency to obtain output data, wherein

each of said plurality of sampling frequency conversion means includes:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an address difference between a writable address and a readable address in said storage means;

and address control means for performing an optimizing ~~a action~~ operation optimizing the address difference detected by said address difference detection means, wherein

said address control means works so as not to execute the optimization operation when the address difference detected by the address difference detector means in each of said plurality of sampling frequency conversion means falls within a predetermined range after passage of a predetermined period of time from a start of supplying said input data, thereby to eliminate a time difference between the output data from said plurality of sampling frequency conversion means.

Claim 9. (Previously Presented) The sampling frequency conversion apparatus according to claim 8, wherein

said predetermined period of time is longer than a time required for stabilizing a ratio between the first sampling frequency of the input data and the second sampling frequency of the output data after a start of supplying the input data.

Claim 10. (Previously Presented) The sampling frequency conversion apparatus according to claim 8, wherein

said address control means performs a control operation to bring said address difference close to a predetermined optimum value when a predetermined period of time has not passed after the start of supplying said input data or when the address difference detected by said address difference detecting means falls outside of the predetermined range.

Claim 11. (Previously Presented) The sampling frequency conversion apparatus according to claim 10, wherein

said address control means executes the control operation by bringing the address difference close to the predetermined optimum value by judging that a moment at which the changing address difference value exceeds the predetermined optimum value or becomes smaller than the predetermined optimum value, is the moment of an optimum address difference.